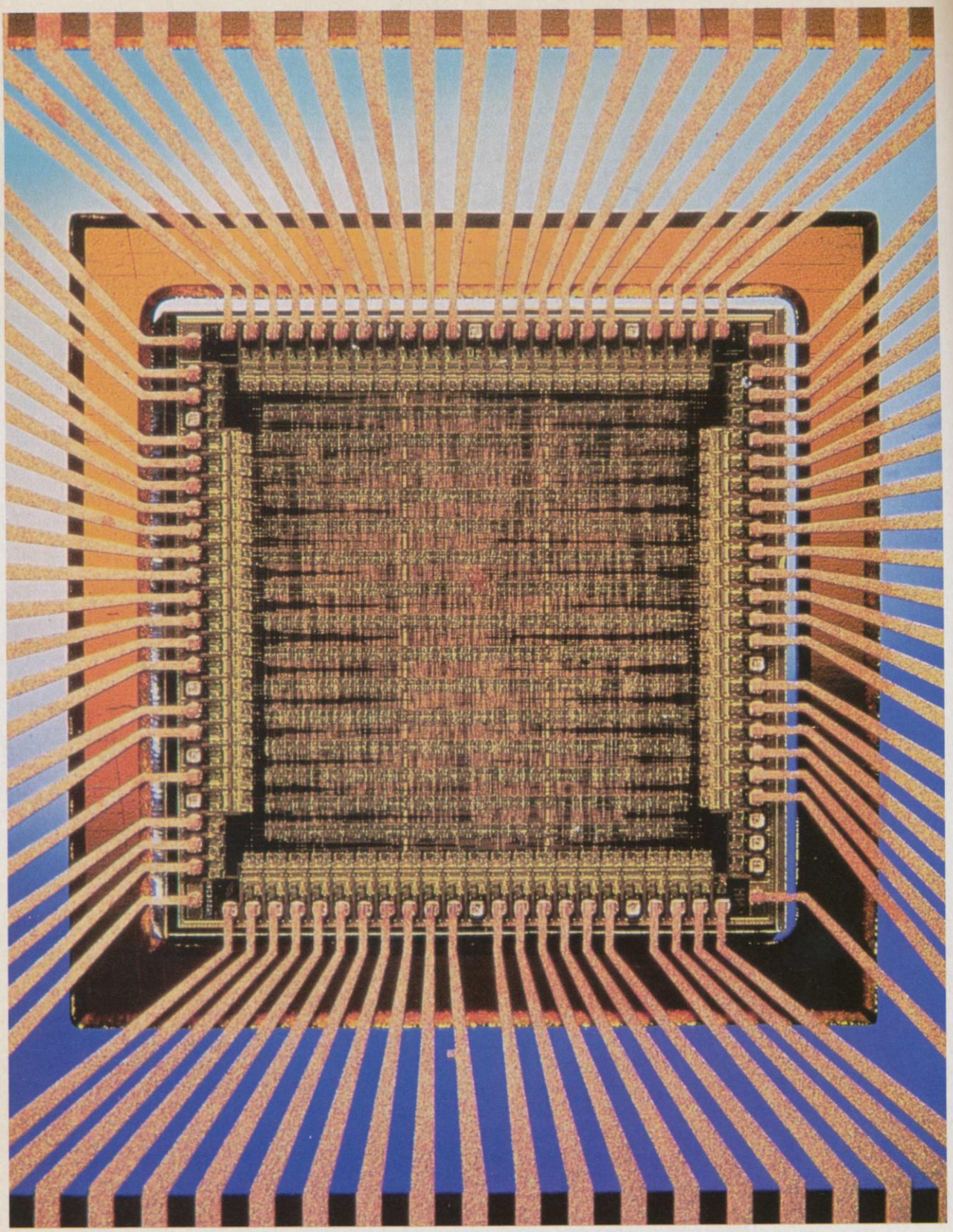

Advanced packaging will play a key role *in the creation of devices and systems in the 1990s. This 84-lead IC resides in a National Semiconductor TapePak package and occupies only 0.36 in² of pc-board space. You can use conventional surface-mount techniques to attach the device to a pc board.*

PART FOUR
DECADE 90
The future of system design

New package technology supports soaring IC and system complexity

The ubiquitous DIP and board-and-backplane technologies have dominated electronic packaging for the last 25 years. However, the growing sophistication of devices and systems signals the decline of such packaging schemes and heralds the arrival of more-advanced techniques for systems designed in the 1990s.

Steven H Leibson, *Regional Editor*

Customers and end users expect electronic systems to become smaller, faster, and more powerful every year; such progress is the hallmark of our industry. The relentless increases in semiconductor integration have played—and will continue to play—a large part in this process, but the next decade's system engineers will also rely on advanced packaging techniques to achieve those size, cost, and performance goals.

Although IC densities increased by six orders of magnitude over the last 25 years, packaging and interconnect technology made only modest gains during that same time. Indeed, because device and system packaging presented few problems for the simpler designs and slower signal rates of the past, packaging technology didn't receive the same attention that IC design did, so it didn't advance in tandem with IC technology. DIPs, for example, went from 14 to only 64 leads, and most engineers continued to use fairly ancient board-and-backplane technologies when designing multicard systems.

These old packaging and interconnection schemes are limiting the speed and complexity of today's advanced systems. Emerging packaging technologies, however, promise to overcome the existing performance barriers by improving electrical characteristics and costs while shrinking board-space requirements. They simply do more with less: They carry higher-frequency signals and handle more interconnections than earlier packaging technologies did, yet use less material.

Packaging issues are now critical to advanced system design, because highly sophisticated electronic systems require increasingly complex interconnection schemes. According to Rent's Rule, an empirical model of system interconnection developed in the 1960s **(Ref 1)**, as chips become more and more complex, they require more leads or pins to connect with the rest of a system. Rent's Rule emphasizes something that engineers now take for granted—that soaring IC complexities demand ever-increasing amounts of interconnection circuitry.

Packaging and interconnect lack pizzazz

Unfortunately, many of the most publicized semiconductor projects dedicated to creating these future ICs don't devote the same level of engineering effort to packaging and interconnection issues that they do to

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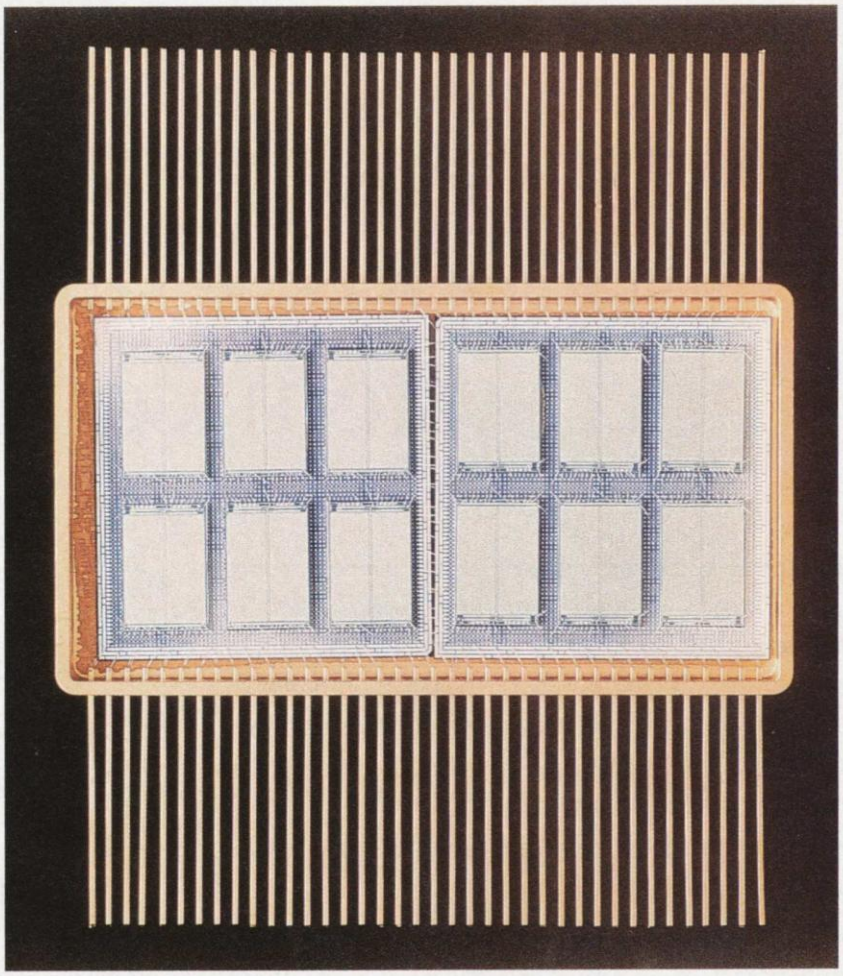


Two silicon circuit boards in a hybrid package *hold twelve 32k×8-bit static RAM chips, creating a 3M-bit, 65-nsec, cache-memory module. (Photo courtesy Mosaic Systems Inc)*

circuit design. According to Robert E Holmes, chief scientist for the Hybrid Components Operation at Tektronix (Beaverton, OR), major projects such as the US government's VHSIC (very-high-speed IC) and MMIC (monolithic microwave IC) programs and the Sematech consortium (in Austin, TX) put "millions of dollars into semiconductor research, but pennies into packaging." Holmes points out that companies wishing to develop new packaging technologies must conduct some basic research: They need to find new materials that solve existing power-dissipation, TCE (thermal coefficient of expansion), and interconnection problems. Funding for such research has been lacking, he says.

Though packaging may not enjoy the same amount of attention as semiconductors do, it's still making progress. For example, surface-mount technology (SMT) is currently forcing systems vendors to revamp their manufacturing processes. SMT replaces board stuffing, which is traditionally a manual process, with very high levels of automation. SMT also effects substantial system size reductions and speed increases. The diminutive SMT packages allow system engineers to shrink existing systems or pack more capabilities into an existing box. The shorter lead lengths of these SMT packages permit faster system operating speeds because they exhibit less resistance, capacitance, and inductance. In addition, the 50-mil lead pitch of SMT packages allows for higher lead counts than conventional through-hole DIPs do.

Because SMT manufacturing represents a major departure from traditional production techniques, US companies have been slow to adopt it. According to

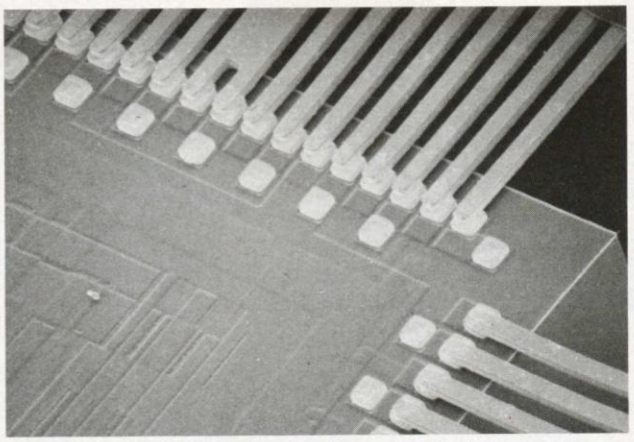


Fig 1—TAB technology allows chip vendors *to bring many more signals off an IC with connections that have lower impedance, more ruggedness, and more reliability than conventional wire bonds provide. In addition, TAB can accommodate ICs with closer pad spacing than wire-bond technology allows. (Photo courtesy Motorola Inc)*

Diane Taylor and Donn Fischer, authors of the book *Surface Mount Technology: A Strategic Report*, 15% of the electronic equipment built in the US during 1985 incorporated SMT. The book predicts that the figure will grow to only 30% by 1990. For Japan, however, those figures are 30% and 50%, respectively.

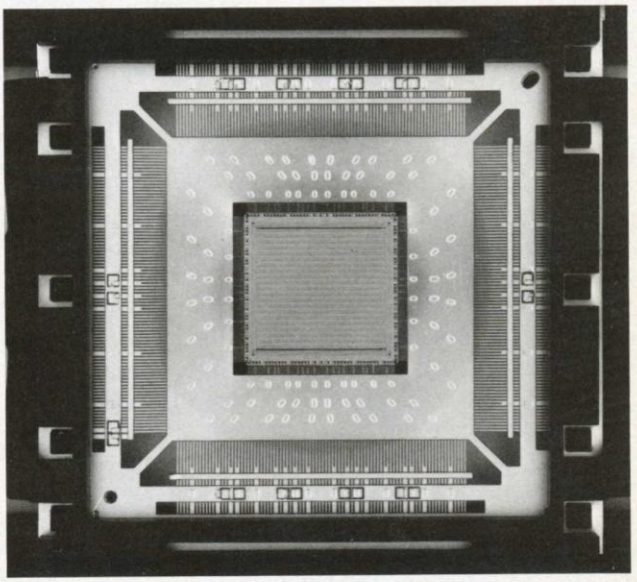
Several of the factors slowing the growth of SMT in the US are a general domestic shortage of SMDs, the incomplete availability of popular logic families in SMD packages, the substantial up-front capital needed for SMT manufacturing equipment, and engineers' inexperience with SMT design techniques. Despite those obstacles, the electronics industry will inevitably convert to SMT manufacturing on a worldwide basis during the 1990s, because by automating production, SMT will let companies produce higher-quality products at a lower cost.

Unfortunately, even today's SMT packages can't achieve the high lead counts forecast for the very dense chips of the 1990s. Currently, plastic leaded chip carriers (PLCCs) have no more than 124 leads, a capacity that falls far short of meeting those future needs. Some advanced ASICs available this year already require more than 500 leads. Even the pin-grid array (PGA)—an expensive and space-consuming package—can't accommodate such devices. To meet high lead-count requirements, packaging engineers are refining an existing package technology: tape-automated bonding (TAB).

Military projects have employed TAB as a high-reliability packaging scheme for more than a decade. TAB improves the reliability of an IC's interconnection by eliminating wire bonds and attaching a tape-based lead frame directly to the silicon die instead **(Fig 1)**. TAB's lead frames have more strength than individually applied, gold wire bonds.

TAB has the potential to become a low-cost packaging technology because gang-bonding equipment can attach high lead-count dies to TAB lead frames much faster than a wire bonder can stitch wires between a chip and a conventional lead frame. Most current TAB packaging schemes, however, employ relatively expensive multilayer film lead frames of copper and polyimide. They also require you to use special equipment for attaching the TAB package to substrates such as pc boards. Therefore, TAB has remained primarily a military technology.

Nevertheless, National Semiconductor (Santa Clara, CA) now uses TAB to construct a low-cost, commercial IC package. The company was investigating inexpensive, reliable, multichip packaging schemes for dynamic-RAM modules and started experimenting with chip-on-board and chip-on-tape approaches to reduce board-space requirements. As a result of this project, National Semiconductor's engineers developed the



TAB packaging accommodates high lead-count devices *such as this 360-lead IC. Currently, TAB handles as many as 500 leads per chip; that figure could reach 1000 during the next decade. (Photo courtesy Motorola Inc)*

TABLE 1—WIRE-BOND VS TAB PACKAGING

	WIRE-BOND PACKAGING						TAB PACKAGING			
	40-LEAD DIP		44-LEAD PLCC		132-LEAD PQFP		40-LEAD TAPEPAK		132-LEAD TAPEPAK	
LEAD TYPE	LONG	SHORT	LONG	SHORT	LONG	SHORT	LONG	SHORT	LONG	SHORT
LEAD LENGTH (IN.)	0.99	0.13	0.20	0.15	0.38	0.26	0.12	0.06	0.31	0.23
RESISTANCE (mΩ)	125	123	98	98	102	101	3.6	2.2	11	8.2
INDUCTANCE (nH)	22	3.9	4.6	3.3	10	7.2	2.1	0.8	6.7	5.1
CAPACITANCE (pF)	0.68	0.12	0.12	0.16	0.21	0.15	0.04	0.02	0.11	0.08

NOTES:
PLCC=PLASTIC LEADED CHIP CARRIER
PQFP=PLASTIC QUAD FLAT PACK
INFORMATION COURTESY NATIONAL SEMICONDUCTOR

TapePak, a TAB packaging technology that combines a single-layer, all-copper lead frame with a molded plastic body and guard ring.

TAB drops lead impedances

TapePak improves connectivity to a die by doing more with less—it replaces bond wires with a short lead frame, greatly reducing lead impedances when compared with similar packages based on wire bonds (**Table 1**). TapePak devices require minimal pc-board space because the molded plastic body is just slightly larger than the die it encloses. National Semiconductor currently offers linear, bipolar devices in TapePak packages, and also plans to put its HPC family of μCs, disk-controller chips, and μP support ICs in TapePak packages. The company has defined four TapePak body styles for ICs with 40 to 360 leads and has obtained JEDEC approval for its 40-, 52-, 68-, and 84-lead designs.

The plastic TapePak body protects the die, unlike military TAB designs, which leave the chip naked and rely on more-expensive ceramic or metal packages for physical ruggedness. TapePak's guard ring protects the IC's delicate leads until the package is attached to a substrate. The ring also delineates a region between the TapePak body and the guard ring, allowing the fine-pitched leads to fan out to test points on 50-mil centers. This feature makes TapePak compatible with existing SMD testers and handlers.

A trim-and-form tool, which attaches to standard pick-and-place machines, allows existing SMT manufacturing equipment to place TapePaks on a board along with other SMDs. Because of TapePak's finer-pitch leads however, the pick-and-place machine must be equipped with a vision-guided placement head. Just before placement, the trim-and-form tool shears off the guard ring and test points and forms the leads into a gull-wing shape. Then the pick-and-place machine's placement head picks up the prepared device and positions it on the pc board. Standard IR or vapor-phase reflow techniques can then solder all the components, whether they're SMD or TapePak devices, simultaneously.

Even though National Semiconductor has tried to make TapePak compatible with existing SMT manufacturing processes, you must still adapt your particular processes to the new package (which you must often do when introducing new SMDs to a manufacturing line). Tom Puza, assistant superintendent of manufacturing engineering at Delco Electronics Corp (Kokomo, IN), says Delco modified all the stages of its SMT manufacturing process (solder printing, device placement, reflow soldering, and repair) to accommodate TapePak. Because of its favorable experiences with the new package, Delco has added TapePak to its package arsenal along with DIPs, 50-mil SMDs, and flip chips (dies that are directly attached to a substrate). Currently, Delco employs TapePak devices in one of its car radios and will use the packaging scheme for other automotive electronic programs in the future.

National Semiconductor is not the only semiconductor vendor that is considering TAB for commercial IC packaging. Motorola Inc (Phoenix, AZ) has licensed the TapePak technology from National Semiconductor and

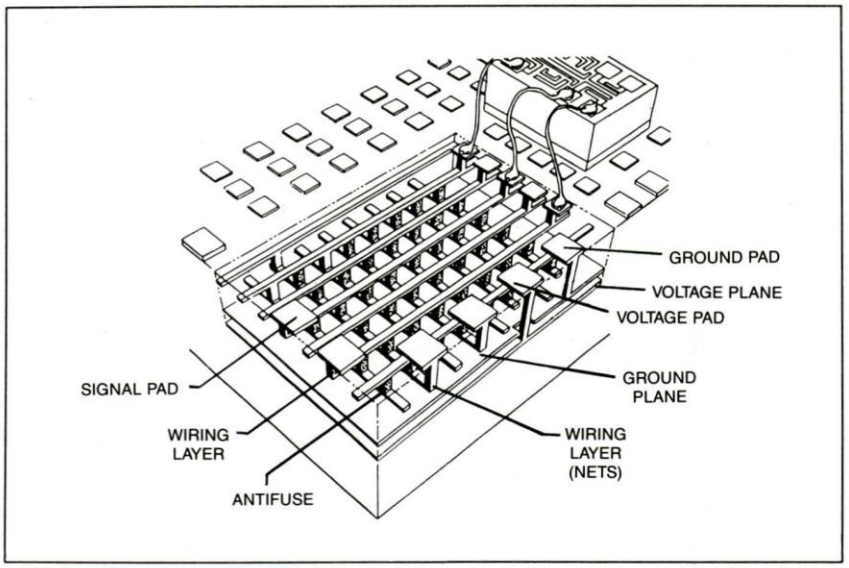


Fig 2—You can create a field-programmable hybrid circuit *by using the silicon circuit board (SCB) from Mosaic Systems Inc: You bond naked IC dies to the SCB and make electrical connections to the SCB's signal, voltage, and ground pads with wire bonds. A 20V programming pulse blows an antifuse linking one trace on the SCB's upper wiring layer to a trace on the lower layer, so you can connect the ICs mounted on the SCB.*

plans to develop its own family of TapePak ICs. Bud Simmons, manager of assembly concepts and methods engineering at Motorola, says that TAB technology such as TapePak can accommodate 500-lead ICs today; he predicts that the technology could be stretched to 1000-lead ICs in the future.

Multichip modules reduce interconnections

You can also use TAB to build multichip subsystems, because a multilayer TAB lead frame closely resembles a multilayer pc board and has similar capabilities for interconnecting ICs. In fact, some companies have already designed such multichip TAB assemblies for military contracts. For example, Texas Instruments (Dallas, TX) used multichip TAB technology to create a 288k-bit memory module for the VHSIC program. The module incorporates four 8k×9-bit static-memory dies. The TAB leads attached to the individual memory dies allowed the company to test each chip and its chip-to-lead interconnections before installing it in the multichip package.

Under another VHSIC contract, Honeywell (Minneapolis, MN) employed multichip TAB technology to create an 18-chip electro-optical image processor that incorporates two 8000-gate CMOS arrays, twelve 16k×4-bit static RAMs, and four glue chips. The entire processor fits into a small, 84-lead package. The company claims that its multichip TAB approach both reduced the image processor's requirement for pc-board space from 96 to 36 cm^2 and cut the board's power consumption to a third by lowering the capacitance of the system interconnections.

Honeywell's image processor contradicts Rent's Rule by showing that, at extremely high integration levels, lead counts may not increase with increasing IC complexity. The processor's 84 leads represent a substantial reduction in system-level interconnection when compared with the total number of pads on the chips that comprise the module. You can see similar reductions in the interconnection requirements of memory modules. For example, the 1M-byte SIMM (single-in-line memory module) reduces the system-level interconnection requirements of nine 20-lead 1M-bit dynamic RAMs—a total of 180 leads—to a mere 30 pins.

Other vendors are also experimenting with exotic multichip packaging schemes in an effort to reduce interconnection requirements at the board or system level. Mosaic Systems Inc (Fremont, CA) manufactures a user-programmable hybrid substrate that it calls the silicon circuit board (SCB). As with ceramic hybrid modules that have existed for decades, you mount bare silicon dies on the SCB's silicon substrate and use conventional wire bonds to wire the I/O pads from the attached dies to signal lines on the SCB. The SCB contains myriad uncommitted signal lines in a 2-layer matrix and provides a field-programmable method of linking those signal lines: To link them, you blow the amorphous-silicon antifuses that occupy most of the intersections in the signal-layer matrix **(Fig 2)**. The company claims that the SCB, depending on its configu-

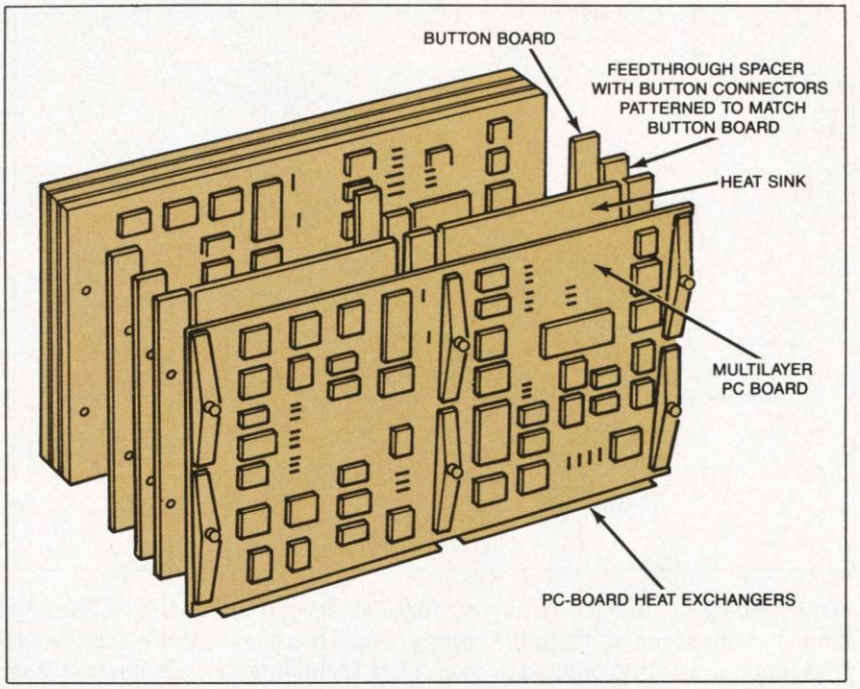


Fig 3—Systems based on the button-board scheme *(which TRW developed for the VHSIC program) simply bolt together without a backplane. The button connectors provide interconnections between the system's pc boards, allowing you to place the circuit boards very close together, which minimizes signal-path lengths. (Figure courtesy TRW* **Quest** *magazine)*

ration, can handle signals with frequencies as high as 200 MHz.

Although a lot of packaging research is directed at device packaging, system packaging must also advance to handle the higher signal frequencies and increased complexity of future electronic systems: Traditional board-and-backplane approaches are reaching their performance limits. Because the conventional backplane topology forces the designer to place all system interconnections at one edge of a pc board, many signals must cover unduly long paths when traveling from one board to another. Long signal paths degrade system performance because they present high capacitive loads to output drivers.

Packaging a system with buttons

New system-packaging schemes are attempting to reduce these long paths. For example, TRW's (Redondo Beach, CA) patented button-connector technology allows signals to jump from board to board at any spot, not just at an edge. The button contact is deceptively simple, resembling nothing more than a miniaturized pad of steel wool. To form a connector, buttons occupy holes etched in a button board made of Photoceram, a material made by Corning Glass (Corning, NY).

You literally bolt a button-board system together, alternating Photoceram button boards with component-carrying circuit boards and topping the assembly off with reaction (pressure) plates (**Fig 3**). The buttons touch associated pads on adjacent pc boards. Button-based systems withstand shock and vibration very well because the entire assembly is under tension from the reaction plates. TRW subjected prototype button systems to 30g vibrations for 12 hours while cycling the temperature of the system and observed no connector failures.

Bob Smolley, TRW's VHSIC assistant project manager and the creator of the button connector, says he developed the buttons in response to TRW's system requirements for the VHSIC program. He says that chips operating at bus speeds exceeding 25 MHz simply can't drive the capacitance of conventional backplanes. The 3-dimensional topology of the button board greatly reduces signal-path lengths and capacitances in comparison with those of 2-dimensional backplane systems. Not only does such an approach allow for increased signal speed, but it also reduces system power requirements, because the electrical power required to drive a signal line is directly proportional to the line capacitance. Smolley says that the button connector's ability to extract a signal from any part of a pc board, not just the edge, can also reduce signal routing, which lets you

reduce board size by as much as 20%.

A 3-dimensional interconnection scheme, developed by Rome Air Development Center (at Griffiss AFB in NY) and Hughes Research Laboratories (Malibu, CA) as part of their investigation of wafer-scale packaging, possibly represents the ultimate in minimal system-interconnect packaging: It uses unpackaged wafer-scale devices and connectorless interconnect technology.

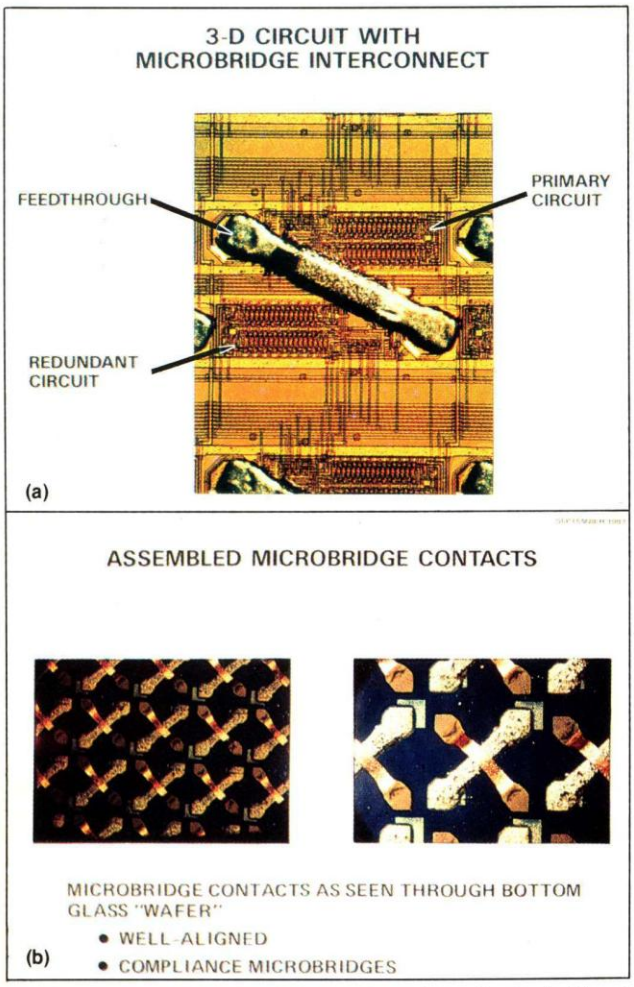


Fig 4—Indium-coated microbridge contacts formed on both sides of a wafer-scale device (a) *allowed Rome Air Development Center and Hughes Research Laboratories to build a system by stacking several wafers. The contacts on top and bottom are orthogonal, so contacts on one wafer touch contacts on the adjacent wafer at only one point* ***(b).*** *Applying compression to the stack slightly deflects the microbridge contacts, creating a high normal force and ensuring good physical contact during reflow soldering. After it's cooled, the soldered stack forms a complete, 3-dimensional computer system, dubbed "the coffee-can computer."*

Using this approach, engineers plate microbridge contacts on both the top and the bottom of each wafer-scale device (**Fig 4**). Feedthroughs, formed in the wafers by dissolving aluminum through the silicon with a high-temperature process, link the microbridge contacts on the top and bottom of a wafer.

After coating these microbridges with indium solder, the researchers created a finished system by stacking several wafer-scale devices so that the microbridges of one wafer contacted microbridges of abutting wafers. Heating the wafer stack while compressing it caused the indium solder to reflow, making the connections permanent and creating a completed assembly. Investigators dubbed this structure "the coffee-can computer" because of its size and configuration.

Microbridge connections create an array of interconnections that run vertically through the wafer stack. Thus, the array topologically resembles TRW's button connector, except that the array is implemented on a smaller scale. Both of these techniques represent minimalist solutions to system-level interconnection. Like these technologies, future packaging and interconnection schemes for both devices and systems will strive to place as little interconnection as possible between the output driver of one IC and the input buffer of the next chip down the line. Such approaches will provide design engineers with the dense, high-speed signal-transmission technology they'll need to build complex systems in the 1990s. **EDN**

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