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Revisiting Decade 90: semiconductor technology

In early 1988, I wrote a five-part series called "Decade 90: the future of system design." In it, I tried to forecast the major technological trends that would shape our industry in the 1990s. In this and the next four editorials, I'll take a look at how close we are to the predicted trends and where we'll be by the end of the decade.

The first installment of Decade 90 looked at the direction of semiconductor technology. In 1988, production quantities of 1-Mbit DRAMs were just starting to become available, setting the practical limit of about 1 million transistors per chip. At that time, advanced optical lithography was creating devices using 1.25-micron feature sizes, and industry experts were saying that optical lithographic techniques would run out of steam at 0.7 micron. "After all, the wavelength of blue light is about 0.5 micron," I wrote. Many semiconductor vendors were looking at more exotic lithographies such as e-beam and X-ray to break the 0.7-micron barrier.

Well, it didn't happen the way the experts predicted. In 1995, we've taken optical lithography to 0.35 micron using tricks such as phase-shift masks. Many semiconductor-fabrication facilities expect to be able to use optical lithography down to 0.1 micron. In that first Decade 90 article, I discussed early IBM experiments that had created a transistor using 0.1-micron geometries. The transistor worked. Since then, other semiconductor vendors, such as Toshiba, have also built 0.1-micron working devices using optical lithography.

Because lithographic developments seem on track in 1995, my 1988 prediction of 1 billion transistors per chip by the end of the 1990s seems certain rather than incredible. Samsung has already built a working prototype of a 256-Mbit DRAM and plans to have the device in production by 1997. That leaves two or three years to quadruple the density to 1 billion transistors per chip before the end of the decade, an event that now seems inevitable.

Because lithographic developments seem on track in 1995, my 1988 prediction of 1 billion transistors per chip by the end of the 1990s seems certain rather than incredible.

The first Decade 90 article closed with a warning: "Current system-design techniques just will not work with tomorrow's IC complexity." And how. The next Decade 90 article covered and my next editorial will tackle changes in electronic-design-automation (then called CAE) tools to accommodate these gargantuan chips.

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Editorial Achievement Award
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1990 Certificate, Best Series
1987, 1981 (2), 1978 (2), 1977, 1976, 1975

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1994, 1991, 1990, 1988, 1983, 1981

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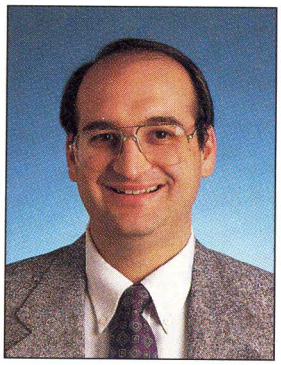

Revisiting Decade 90: EDA tools

In early 1988, I wrote a five-part series called Decade 90: The future of system design. *In it, I tried to forecast the major technological trends that would shape our industry in the 1990s. This is the second in a series of five editorials looking at how accurate the predictions were.*

Decade 90's prediction of one billion transistors per chip by the end of the 1990s posed a big problem: managing large designs. The second Decade 90 article looked at CAE tools. In 1988, most system designers used schematic-drafting tools to design even large ICs, such as ASICs. HDLs were just starting to come into vogue. The article discussed using Mentor Graphics' tools (pre-VHDL) to create a 9000-gate ASIC, but the tools ran out of steam above 20,000 gates.

By 1988, VHDL had been developed—but it lacked even one good simulator.

Today you can get several hundred thousand gates on an ASIC, PLDs are breaking through the 20,000-gate level, and schematic-drafting EDA tools cannot take you to those levels easily. You've got to work at higher levels of abstraction to design chips that large. As predicted in the article, HDLs moved into place to fill this need.

Back in 1988, Gateway's (now Cadence's) Verilog held the lead in HDLs. VHDL had been developed, but it lacked even one good simulator according to a director of VHSIC programs at TRW. The article also mentioned competing HDLs, such as Aida's ADL and Endot's ISP'. Today, Verilog continues to enjoy substantial product support from several companies, and VHDL now has more than one "good simulator."

In 1998, electronic-system-design-automation (ESDA) tools had yet to appear, but the article discussed ADAS, a system-level development tool from the Research Triangle Institute. You could design and simulate systems with ADAS, but the tool didn't emit an HDL description of your system for further development, as today's ESDA tools can.

Spice also popped up in that 1988 article, as a tool for developing backplanes. Today, Spice has become a system designer's tool that's a requirement for developing submicron ASICs. Below 0.5 microns, transistor characteristics go wacky, and simple device-characteristic approximations won't allow you to take maximum advantage of the silicon.

The article concluded by stating that companies that failed to adopt CAE tools would find themselves at a competitive disadvantage. From a 1995 perspective, that was a gross understatement.

Steven H. Leibson

EDITOR IN CHIEF

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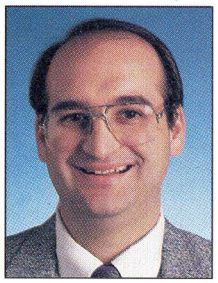
Revisiting Decade 90: Design for Test



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You could probably say that system designers don't like design for test (DFT) any better in 1995 than they did in 1988, for the same reasons. DFT techniques take extra time, slap a performance penalty on the design, and eat up precious silicon that could be used to provide other features. Nevertheless, designers **are** using DFT techniques more now than in 1988. For example, about 60% of LSI Logic's ASIC design starts now incorporate boundary scan. With big ASIC designs, DFT may be the only way to make the initial design verification of a working 100,000-gate ASIC; the ability to test the ASIC in manufacturing is gravy.

Back in 1988, it was becoming clear that board-level manufacturing technologies such as surface-mount technology (SMT) made bed-of-nails board testing nearly impossible. Today, we build almost everything using SMT, and multichip modules are delivering still smaller, even more untestable geometries.

In 1988, Paul Gifford, manager of central systems engineering at Sequent Computers, estimated that the DFT performance penalty was 5 or 6%. It's even lower now, but, for some designs, any speed penalty was and is unacceptable. Some things don't change over time. However, with several million transistors available on large chips, a few thousand dedicated to test don't seem onerous.

The Joint Test Action Group (JTAG) was already creating the serial-test standard in 1988. It now exists as the IEEE-1149 Standard, and many semiconductor vendors have pressed it into service for other features, such as device programming. Although you can now get many standard ICs and ASIC macros with JTAG ports, its use is still far from widespread.

One test technique, I_{DDQ}, didn't appear in the 1988 Decade 90 article, but it now has a growing number or proponents. One major reason for its growing popularity is that it's an after-the-fact test. Feed the chip a few carefully selected test vectors, watch how its current consumption jumps, and mark it faulty if its current consumption doesn't jump to the right tune. You don't have to use DFT if you use I_{DDQ}, a feature sure to win the hearts of harried system designers.

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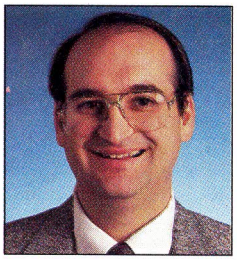
Revisiting Decade 90: packaging



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The fourth "Decade 90" article addressed new packaging technology for the electronics industry. In this article, you could find every major packaging trend that has now come to dominate the industry. The article opened with a full-page shot of a National Semiconductor IC in a tape-automated bonding (TAB) package. True, few ICs today come in TAB packages, but, with the introduction of Intel's 75-MHz Pentium μP in TAB, you'd have to call the technology mainstream. Incidentally, Epson has been packaging Intel's 80386 and 80486 μPs in TAB packages for years in the Cardio PC-in-a-credit-card products. The high pin counts and low lead impedances of TAB technology suit it well to today's dense, high-speed circuits.

Similarly, "Decade 90" discussed multichip modules (MCMs), which have become far more common today than they were in 1988. A silicon-on-silicon MCM technology developed by Mosaic Systems looked very advanced in 1988, but Ross Technology's HyperSPARC multidie package uses a silicon-substrate, silicon-on-silicon MCM technology. This technique allowed the company to pack a 110-MHz, 6-million-transistor CMOS processor with 256 kbytes of second-level cache memory into one 131-pin PGA package. It's still not cheap, but this processor is for high-end workstations, not high-end military or space hardware.

My favorite packaging technology of the future was the coffee-can computer developed at the Rome Air Development Center (at Griffiss Air Force Base, New York). This technology took whole wafers, deposited solder-covered gold microbridges across their tops and bottoms, and then created a system by stacking, compressing, and heating several wafers. The contacting microbridges made the connections between wafers. No, we don't see that exotic 3-D, wafer-scale chip-packaging technology in use today, but we certainly do see 3-D chip-packaging technology routinely in use at companies such as Densepac Microsystems and Electronic Designs Inc. These companies use the technique to boost the densities of memory ICs beyond what today's monolithic fabrication technology can produce.

Clearly, the advances I forecast in the "Decade 90" packaging article all came to pass before we made it halfway through the decade. IC speeds, power-dissipation requirements, and pin densities continue to press packaging designers, who continue to develop innovations, such as copper heat spreaders and ball-grid arrays. Surface-mount-package lead pitches continue to shrink (coincidentally all but wiping out the electronic hobby industry, but that's another editorial). Somehow, we've stuck by the indomitable edge connector—even with today's "hot" PCI bus—but there are a few alternatives, such as board-stacking connectors and two-piece connectors.

The future of electronic packaging from here to the end of the decade isn't nearly as clear. Today's IC packages seem able to handle incredible densities, such as Ross Technology's HyperSPARC processor, and high speeds, such as the 500-MHz Rambus technology. It may be that we have all the packaging technology we need for the next five years, but I wouldn't count on that.

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Steven H. Leibson

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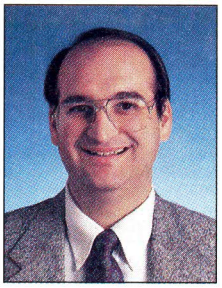
Revisiting Decade 90: fault-tolerant design



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Military and aerospace systems have used and continue to use fault-tolerant designs, but commercial, industrial, and consumer products have not followed, for three reasons. First, the reliability of conventional electronic hardware is constantly improving, so the added cost and complexity of fault-tolerant design is unwarranted. Processors have MTBF ratings in the hundreds of years, and memories no longer suffer as much from soft errors. Further, increasing levels of integration have ushered in the era of single-chip systems, and surface-mount assembly with its automated production has caused a tremendous improvement in large-system reliability. Sensor-based feedback systems compensate for wear and tear without resorting to redundant fault-tolerant design.

Second, the increasing pace of innovation in the electronics industry has dramatically shortened the useful life of most electronic products. Five-year life cycles have become the exception. In fact, newer, more efficient electronic equipment comes along to replace older units before the older units reach the end of the constantly receding reliability curve. Companies must either ride the technological wave by constantly upgrading equipment or wipe out and let the competition overtake them.

Third, the competitive '90s attitude precludes companies from employing design strategies that add cost but not "value." Few customers are willing to pay substantially more money for unstoppable hardware, but many will pay extra for more performance. For example, fault-tolerant design has taken hold in the market for redundant arrays of inexpensive disks (RAID) (*EDN*, Nov 24, 1994, pg 81). RAID systems gang multiple hard-disk drives, thus realizing the combined benefits of higher throughput and fault tolerance. Because disk drives are electromechanical, they are less reliable than are purely electronic systems. As such, disk subsystems can benefit from fault-tolerant design techniques. Even hard-disk reliability has skyrocketed in the last couple of years, however. Fault tolerance has succeeded in RAID designs but failed to catch on elsewhere because RAID is one application in which fault tolerance also delivers improved performance, thus providing sufficient value to justify the expense. (I was not farsighted enough to mention RAID in my "Decade 90" article on fault tolerance.)

If you've been keeping score over these last five editorials, you may have noticed that the "Decade 90" series did a good job of predicting development, at least from the mid-decade perspective. Although we've seen a lot of innovation, many things haven't changed. ICs still use transistors—albeit much smaller transistors these days—and digital circuits still employ binary coding and signaling schemes. We still solder ICs to circuit boards, though through-hole technology is rapidly going the way of tube sockets and discrete, handcrafted wiring.

I'm not prepared to write a "Millennium 3" series of prognostications just yet, but I will point out a few interesting and revolutionary developments on the horizon. Quantum-line and -dot semiconductors and polymer (plastic) transistors are already working in laboratories. K Eric Drexler's visions of nanomachines increasingly haunt my dreams, spelling the possible end of the electronics age (at least as we know it) early in the next century. The one black hole in all of this future tech is software. I don't care what the object-oriented advocates say; we're still in the software Stone Age. No matter what technology we use to build hardware, software will be around for a while.

If you have any insights into the Third Millennium, I'd be interested in hearing from you.

Steven A. Leibson

EDITOR IN CHIEF

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